

8253/54 Timer

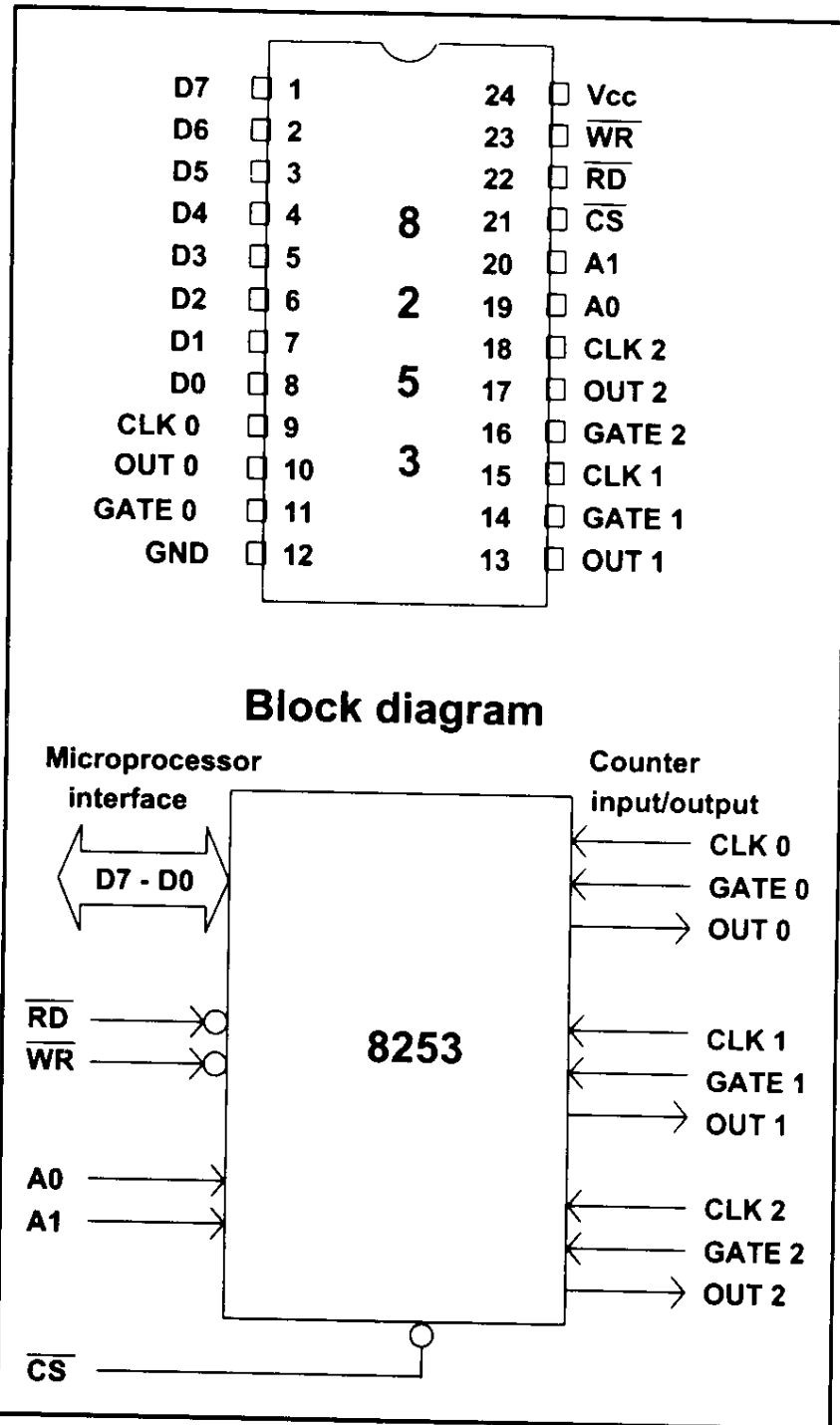


Figure 13-1. 8253 Pin and Function Diagram
 (Reprinted by permission of Intel Corporation, Copyright Intel Corp. 1983)

Addressing the 8253/54

Table 13-1: Addressing 8253/54

$\overline{\text{CS}}$	A1	A0	Port
0	0	0	Counter 0
0	0	1	Counter 1
0	1	0	Counter 2
0	1	1	Control register
1	x	x	8253/54 is not selected

(Reprinted by permission of Intel Corporation, Copyright Intel Corp. 1983)

8253/54 Control Word

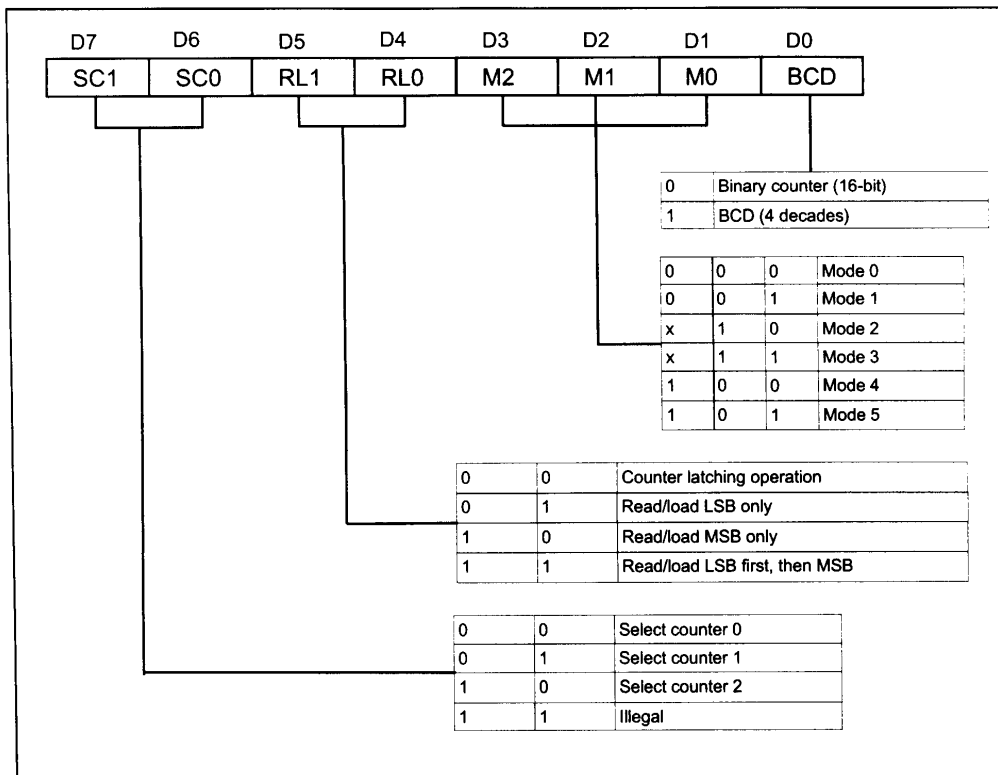


Figure 13-2. 8253/54 Control Word Format
(Reprinted by permission of Intel Corporation, Copyright Intel Corp. 1983)

8253/54 Operating Modes

- Mode 0 Interrupt on terminal count
- Mode 1 Programmable one shot
- Mode 2 Rate Generator
- Mode 3 Square wave rate Generator
- Mode 4 Software triggered strobe
- Mode 5 Hardware triggered strobe

8253/54 Connections in the PC

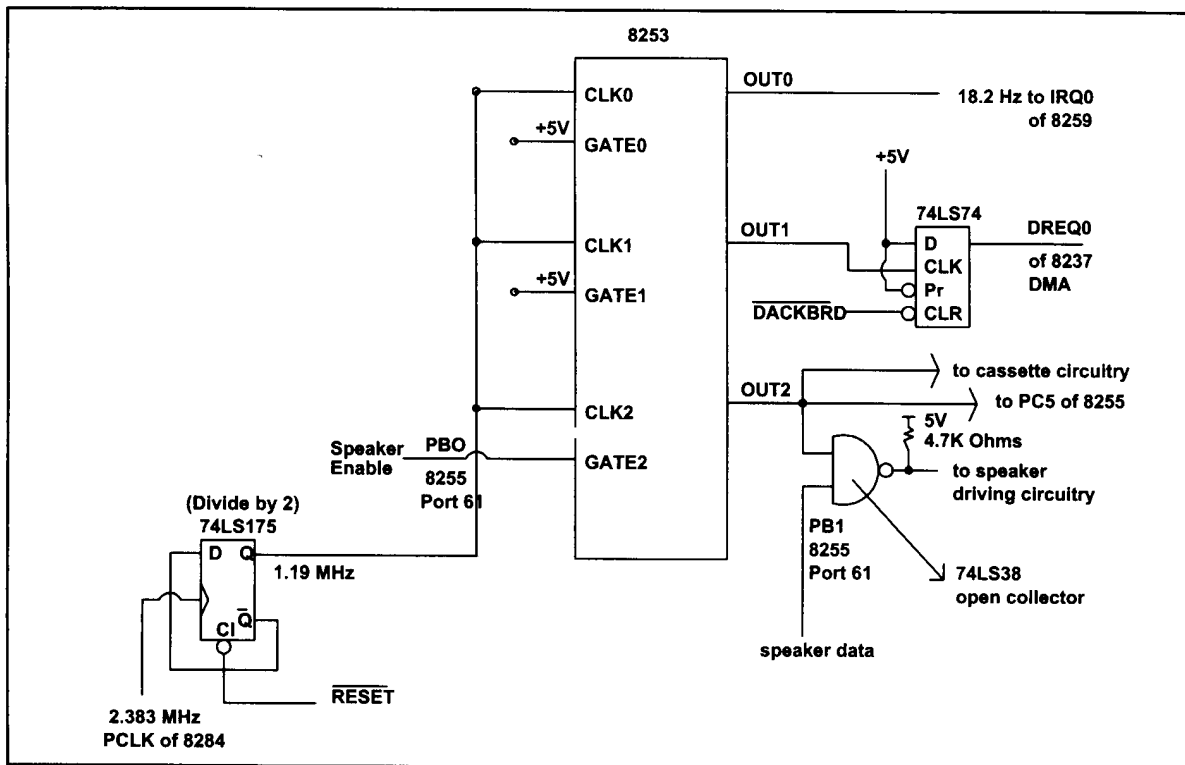


Figure 13-4. 8253 Chip Connections in the PC

Initializing the 8254 timer chip

```
TMR_CONTROL    EQU    43H
TMR_COUNTER0   EQU    40H
TMR_COUNTER1   EQU    41H
TMR_COUNTER2   EQU    42H
```

```
*****
;INIT_TMR
; This procedure intializes the 8254 on the motherboard and programs
; counter 0 to generate a pulse every 65,536 clock ticks
;*****
```

```
INIT_TMR      PROC FAR

                PUSH AX

                MOV  AL, 00110110B    ; control register
                OUT  TMR_CONTROL, AL

                MOV  AL, 00000000B    ; LSB of clock divisor
                OUT  TMR_COUNTER0, AL

                MOV  AL, 00000000B    ; MSB of clock divisor
                OUT  TMR_COUNTER0, AL

                MOV  AL, 01010100B    ; control register
                OUT  TMR_CONTROL, AL

                MOV  AL, 18           ; LSB only clock divisor
                OUT  TMR_COUNTER1, AL

                POP  AX
                RET
INIT_TMR      ENDP
```