



# Intel® 82443MX PCIset

## Specification Update

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*April 2001*

**Notice:** The Intel® 82443MX PCIset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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## Revision History

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Date of Revision	Revision	Description
6/22/99	-001	Document includes all known specifications to date (original version).
9/18/99	-002	Added Erratum #32 Added workarounds to Errata #30 and #31
01/18/99	-003	Added Erratum #33 Added Document Changes #1, #2 and #3
08/18/00	-004	Added Erratum #34 and #35
03/06/2001	-005	Added Erratum #36 Updated Errata #33 - Removed workaround option #3 (Option #3 will be revised in Q2 2001 release of 440MX Specification Update for USB high-speed device compatibility.)

## Preface

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This document is an update to the specifications contained in the Intel® 82443MX PCIset Datasheet and other documents related to the 82443MX PCIset. It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel 82443MX PCIset behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Note:** Errata remain in the specification update throughout the product's lifecycle or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or documentation.

## Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 82443MX PCIsset steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Shaded:	This item is either new or modified from the previous version of the document.
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## Errata

Number	Stepping(s)		Page	Status	Errata
	A-0	B-0			
1	X		8	Fixed	AC'97 Multifunction Configuration not recognized
2	X		8	Fixed	AC'97 Dynamic Clock Gating corrupts data
3	X		9	Fixed	AC'97 Cold Reset does not clear Codec Access Semaphore Bit and Read Completion Bit
4	X		9	Fixed	SMI/SCI for Wake-on-Ring not generated in Dual Codec System
5	X		10	Fixed	SDRAM Leadoff Command Timing must be set to 4 CPU Clocks
6	X	X	10	NoFix <sup>1</sup>	C3 Power State/BMIDE and Type-F DMA Livelock
7	X	X	10	NoFix	Device Monitor 9 and accesses to IO locations 62/66h
8	X		13	Fixed <sup>2</sup>	USB Port Enable and Post Status Bits
9	X		13	Fixed	C3/POS/STR Memory Hang condition
10	X		14	Fixed	SUSTAT1# Implemented as SUSTAT#
11	X	X	14	No Fix	ISA Verify followed by PCPCI DMA
12	X		14	Fixed	USB Dribble
13	X		15	Fixed	IDE PREFETCH

14	X	X	15	NoFix	PCI accesses to External PCI-based IDE Devices will not cause Power Management events
15	X	X	16	NoFix	Burst Events may cause LVL2 or LVL3 register reads to be missed
16	X	X	17	NoFix	Device Trap
17	X	X	17	NoFix	Daylight Savings Time Errata
18	X		17	Fixed	Native Audio Bus Master Base Address
19	X		18	Fixed	Native Audio Bus Master Base Address
20	X		18	Fixed	AC_RSTB Errata
21	X	X	18	NoFix <sup>2</sup>	Boundary Condition issues for USB Connects and Disconnects
22	X		20	Fixed	Incorrect Data transmitted through AC'97 Modem Out Channel
23	X		20	Fixed	Port Enable/Disable Change Bit incorrectly Set for OC# Assertion During S1-S5 States
24	X	X	21	NoFix	Minimum latency to access USB I/O Registers after exiting from Suspend
25	X		21	Fixed	USB Transaction initiated without Ample Time to complete
26	X		21	Fixed	Mismatched PIDs Lead to False Bus Cycle
27	X	X	22	NoFix	Native Modem Bus Master Base Address
28	X	X	22	NoFix	AC'97 PCM Out
29		X	23	NoFix	Incorrect Recognition of High/Low speed USB device out of Resume
30		X	23	NoFix	Power Management General Purpose Status Register "USB_STS" bit not Cleared Correctly
31		X	24	NoFix	USB Port Status and Control Register "Connect Status Change" bit Incorrectly Set
32	X	X	25	NoFix	USB Rise/Fall Time Matching
33	X	X	25	NoFix	USB Connect Status Change Bit does not get set under certain conditions.
34		X	31	NoFix	AC97 Soft Audio and Soft Modem Issue during Intel® SpeedStep™ Technology Operating Mode Transitions
35		X	32	NoFix	GPIO22/PIRQC# and GPIO23/PIRQD# Errata
36		X	32	NoFix	AC'97 Master Abort Errata

**NOTES:**

1. This erratum will be fixed only for BMIDE in B-0 stepping.
2. Fixed for certain boundary conditions. See Erratum #21 for details.

## Specification Changes

Number	Stepping(s)		Page	Status	Specification Changes
	A-0	B-0			
N/A			28		None in this specification update revision

## Specification Clarifications

Number	Stepping(s)		Page	Status	Specification Clarifications
	A-0	B-0			
N/A			29		None in this specification update revision

## Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
1		30		GTL VREF Document Correction for Intel® 82443MX PCISet Electrical and Thermal Specification
2		30		PME# Signal Description Correction
3		30		Thermal Design Power Change for 66-MHz Operation



## Identification Information

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This section covers the Intel® 82443MX PCIset.

### Intel 82443MX PCIset Marking Information

Stepping	Host Bus/SDRAM Frequency	Package	Top Marking	Notes
A-0	66	BGA	FW82443MX Q702ES	Engineering Sample
B-0	66	BGA	FW82443MX Q728ES	Engineering Sample
B-0	66	BGA	FW82443MX SL37L	Production Units
B-0	100	BGA	FW82443MX100 SL3N4	Production Units

## ***Specification Changes***

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There are no specification changes.

# Errata

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## 1. Multifunction Configuration Not Recognized

**Issue:** AC'97 Audio/Modem PCI Functions can not be seen by the operating system because the chipset read-only multi-function bit (bit 7) in the Header Type Register (Device 0, Function 0, Register 0Eh) is incorrectly set to "0." Since a setting of "0" indicates a single function device, operating systems are unable to recognize both audio and modem PCI functions.

**Implication:** Operating system drivers will not enable audio/modem functionality through AC Link when this bit is set to "0."

**Note:** The 440MX systems using PCI Audio/Modem are not affected.

**Workaround:** The BIOS must alter the setting of the multifunction bit in the Header Type Register to return "80h" when read. This will allow AC'97 function 1 and function 2 to be assessable when the OS or driver calls those PCI BIOS functions. The following three PCI BIOS function calls need to be modified in both 16-bit and 32-bit services:

1. ax=B108: Read\_Config\_byte
2. ax=B109: Read\_Config\_word
3. ax=B10A: Read\_Config\_dword

**Status:** Fixed in B-0 stepping.

## 2. AC'97 Dynamic Clock Gating Corrupts Data

**Background:** The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream and contains valid data. If a slot is "tagged" invalid, then it is the responsibility of the source of the data (AC'97 for the input stream and AC'97 controller for the output stream) to stuff all bit positions with "0's" during that slot's active time. SYNC remains high for a total duration of 16 BIT\_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase." The remainder of the audio frame where SYNC is low is defined as the "Data Phase."

**Issue:** When the power management feature dynamic clock gating is enabled, outgoing AC'97 data slots 3, 4, and 5 will be corrupted. Dynamic clock gating is enabled by setting the GCLKEN bit in the Power Management Control Register (Device 0, Function 0, Register 7Ah) to a "1." The operation of the other functions remains unaffected.

**Implication:** The 440MX based platforms using audio, modem, or audio/modem through the AC Link will be affected with data corruption in slots 3, 4, and 5. Designs using PCI based audio, modem, or audio/modem are unaffected.

**Workaround:** The BIOS must disable the Gated Clock Enable (GCLKEN), bit 2, in the Power Management Control Register (PMCR).

**Status:** This erratum only affects stepping A0 and will be fixed in stepping B0.

### 3. AC'97 Cold Reset Does Not Clear Codec Access Semaphore Bit and Read Completion Bit

**Issue:** An AC'97 Cold Reset does not clear the Codec Access Semaphore bit and Read Completion bit. The Cold Reset bit is located at bit 1 of the Global Control, the Codec Access Semaphore bit is located at bit 0 of the Codec Access Semaphore Register, and the Read Completion bit is located at bit 15 of the Global Status Register.

**Implication:** The AC'97 driver will not be able to use the AC'97 controller if it thinks the Codec is busy with the Semaphore bit set.

**Workaround:** Do not issue a Cold Reset command when the Codec Access Semaphore bit or the Read Completion bit is set. All I/O transactions should be completed before attempting to issue a cold reset. The AC'97 controller will clear the semaphore bit upon completion of the I/O transaction. The AC'97 driver should also clear the Read Completion bit before issuing a cold reset.

**Status:** This erratum only affects stepping A0 and will be fixed in stepping B0.

### 4. SMI/SCI for Wake-on-Ring Not Generated in Dual Codec System

**Issue:** In a dual codec system, the 440MX will not generate a SMI/SCI for Wake-on-Ring required to load the modem driver (which has been unloaded when the modem codec transitioned to the D3 state) when audio codec is alive (and therefore AC Link is active).

**Implication:** This prevents proper wakeup via AC'97 protocol.

**Workaround:** None.

**Status:** Fixed in B-0 stepping.

### 5. SDRAM Leadoff Command Timing Must Be Set to Four CPU Clocks

**Issue:** Timing issues exist when the Leadoff Command Timing (LCT) bit, bit 3 in the SDRAM Control Register (Device 0, Function 0, Register 76-77h), is programmed to a "1." This corresponds to a CS# leadoff time of three CPU clocks.

**Implication:** A CS# leadoff time of 3 is not allowed.

**Workaround:** Program the LCT bit to "0", which corresponds to a CS# leadoff time of four CPU clocks.

**Status:** Fixed in B-0 stepping.

### 6. C3 Power State/BMIDE and Type-F DMA Livelock

**Issue:** The 440MX will not always correctly reflect BMIDE and Type-F DMA activity on the BMSTS bit in the Power Management Status Register (PMSTS) of the 440MX Function 3.

**Implication:** When the OS enters a C3 state, it will disable the arbiter and then perform a PLVL3 register read to enter the C3 state, causing LIVELOCK to occur and resulting in a system hang.

**Workaround:** In the OS initialization code, DISABLE Type-F DMA if BIOS indicates C3 support. If BIOS indicates that C3 is not supported, leave Type-F DMA enabled. Note that this workaround is only for Type-F DMA and that there is no workaround for BMIDE.

**Status:** This erratum will be fixed for BMIDE in B-0 stepping. The workaround must be implemented for Type-F DMA.

**Note:** This erratum was carried over from the Intel® 82371EB (PIIX4E).

## 7. Device Monitor 9 and Accesses to IO Locations 62/66h

**Issue:** If Device 9 Idle Enable (IDL\_EN\_DEV9), Burst Reload Enable (BRLD\_EN\_DEV9), or Global Reload Enable (GRLD\_EN\_DEV9) bits are set, then the idle, burst, or global standby timer will reload for I/O accesses to ISA Legacy addresses 62 or 66h. This is regardless of the Generic Decode Monitor Enable bit setting (GDEC\_MON\_DEV9).

If Device 9 Trap Enable bit (TRP\_EN\_DEV9) is set, the 440MX generates a trap SMI for accesses to ISA Legacy addresses 62 or 66h. This is regardless of the Generic Decode Monitor Enable bit setting (GDEC\_MON\_DEV9) and the value of the Programmable Base Address and Programmable Mask register settings (BASE\_DEV9 and MASK\_DEV9).

**Implication:** Device 9 cannot be used as a monitor for I/O device addresses exclusive of 62 and 66h. GPI4 can not be used exclusively to reload the idle, burst, or global standby timers because accesses to ISA Legacy addresses 62 or 66h will also reload the times.

**Note:** GPI4 is still available as a General Purpose Input.

**Workaround:** None. If a generic I/O device monitor exclusive of I/O address 62 and 66h is needed, then use Device 10 if it is available.

**Status:** This will not be fixed in future steppings of the 440MX.

**Note:** This erratum was carried over from the Intel® 82371EB (PIIX4E).

## 8. USB Port Enable and Post Status Bits

**Issue:** A boundary condition can occur while the 440MX is entering a POSCL, STR, STD, or SOFF suspend state and a USB wake event occurs. When the 440MX resumes from POSCL, STR, STD, or SOFF the port enable and port status bits are no longer set. These bits are in the Port Status and Control Register (PORTSC).

**Implication:** The OS or application may no longer be able to use USB.

**Workaround:** None.

**Status:** Fixed in B-0 stepping.

## 9. C3/POS/STR Memory Hang Condition

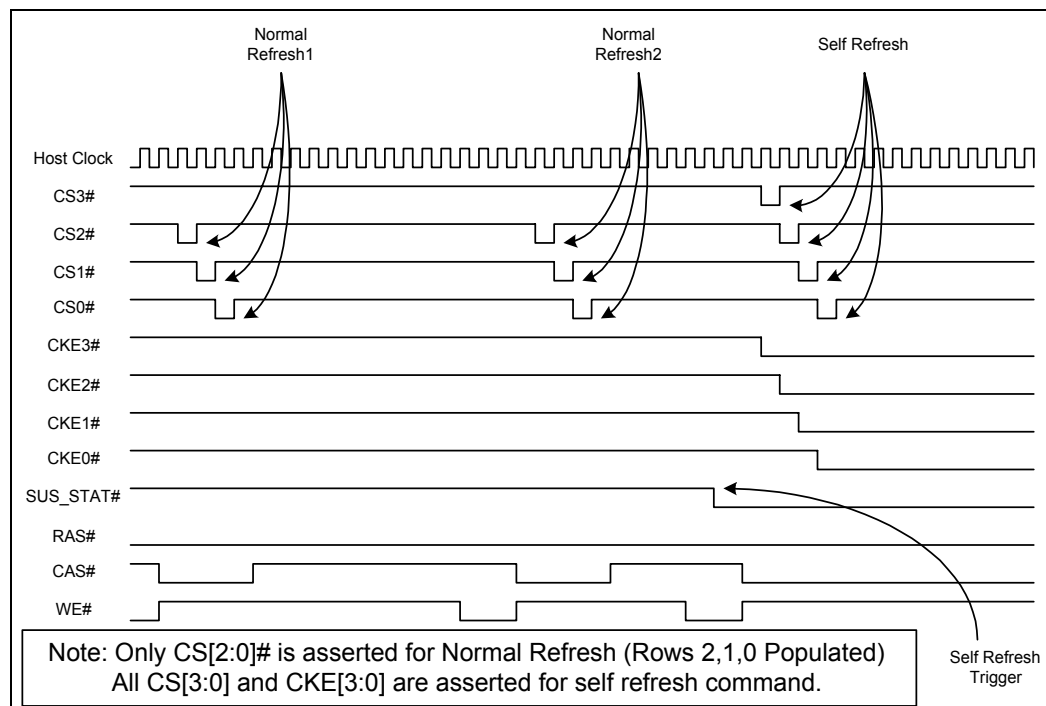
**Issue:** SDRAM may be prevented from being put into self-refresh state when a self-refresh entry request triggered by SUS\_STAT# assertion collides with a normal refresh caused by internal timer expiration. The collision between the two requests results in anomalous behavior on the CS[0-3]# and CKE[0-4]#, which can cause the system hang/memory corruption. There is a three Host clock window in which the assertion of SUS\_STAT# can cause this failure.

The following describes both a successful self-refresh entry and an unsuccessful self-refresh entry.

Figure 1 illustrates a successful suspend entry sequence for a system which has rows 0, 1, and 2 populated. Note that for normal refresh, only the chip selects for the populated rows are asserted,

whereas for the self-entry command, all four chip selects are asserted regardless of its population. Assume that dynamic SDRAM power-down feature is disabled. If all four rows are populated, it is impossible to capture this erratum.

**Figure 1: Successful Self-refresh Entry**

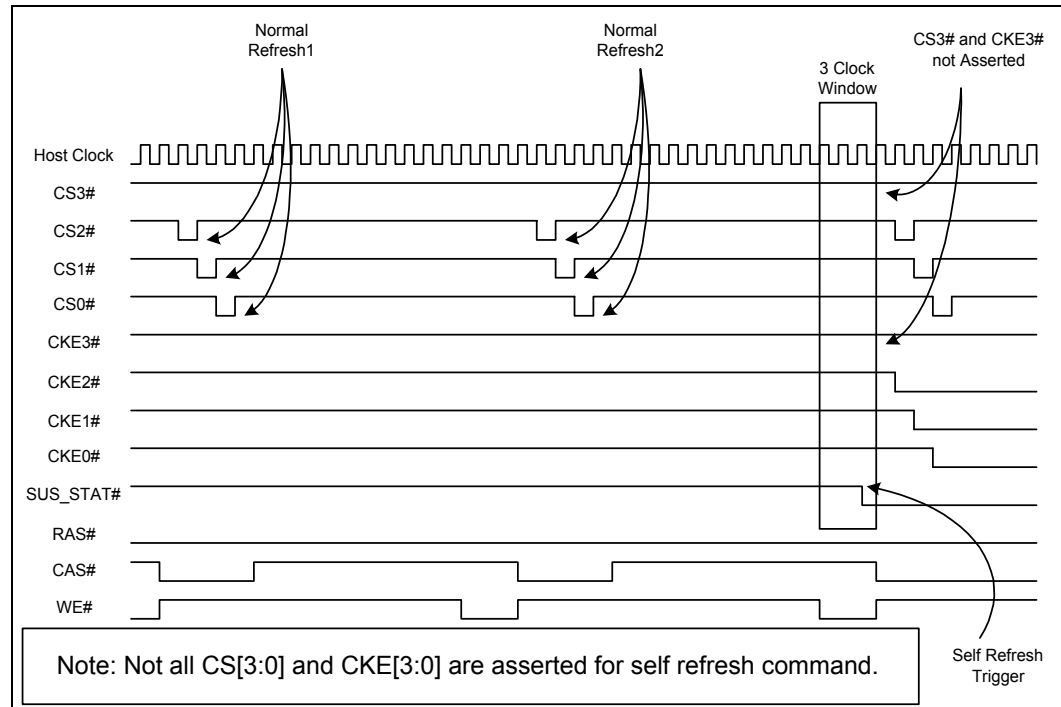


An unsuccessful self-refresh will exhibit the following characteristics:

1. SUS\_STAT# assertion is taking place around a normal refresh request.
2. CS# and CKE# signals are asserted only for the populated rows.

Figure 2 illustrates an unsuccessful self-refresh entry sequence. Note that SUS\_STAT# is being asserted approximately the same time that the third normal refresh would have taken place. Since the SUS\_STAT# assertion hits the three host clock window, CS3# and CKE3# do not get asserted during the self-refresh entry sequence.

Figure 2: Unsuccessful Self-refresh Entry



**Implication:** The system may hang if an unsuccessful self refresh entry sequence occurs.

**Workaround:** Please refer to the SDRAM Suspend Refresh Erratum APM Workaround Write-up, Rev 1.0 for a software workaround solution.

**Status:** Fixed in B-0 stepping.

**Note:** This erratum was carried over from the Intel® 82443BX AGPset.

## 10. SUSTAT# Implemented Incorrectly

**Issue:** SUSTAT# normally notifies peripheral devices (Graphic or Cardbus controllers) during POS, POSCCL, POSCL, or STR states. The current implementation of SUSTAT# notifies peripheral devices during POS, POSCCL, POSCL, STR, or C3 states.

**Implication:** SUSTAT# will be incorrectly asserted in C3.

**Workaround:** Please contact Intel for partial solutions.

**Status:** Fixed in B-0 stepping.

## 11. ISA Verify Followed by PCPCI DMA

**Issue:** Upon completion of an ISA Verify Mode cycle that reaches Terminal Count (TC), the 440MX will not transition an internal TC signal from the TC state to the Idle state.

**Implication:** If a PCPCI DMA cycle follows an ISA DMA Verify cycle that reaches terminal count with no other DMA, ISA Master, or ISA Refresh cycles between them, then the 440MX will assert the TC signal on the first data transfer of the PCPCI DMA cycle. This results in an incomplete data transfer.

**Workaround:** None.

**Status:** This will not be fixed in future steppings of the 440MX.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.

## 12. USB Dribble

**Issue:** A USB receive packet with a bitstuff following the transmission of CRC, coupled with a dribble bit due to prop delays through cables and HUBs, may be incorrectly interpreted by the USB host controller state machine as a poorly formed EOP.

**Implication:** The host controller response to this is a non-acknowledge with a CRC/Timeout status communicated to the software. If this condition persists, the error count associated with this packet will be exceeded and an interrupt can be generated to software. This will stall the USB device. Current software reports a device error to the user via a pop-up window. Another implication is that the installed base may have limited USB expandability via HUBs.

**Workaround:** There are two possible workarounds.

1. Hardware: Attach the USB device into a USB port closer to the root hub.
2. Software: Detect the CRC/Timeout error and count exceeded and attempt to re-queue the packets while changing the length of the packets. Changing the length of the packets will change the CRC and thus will likely remove the combination of the two events causing the failure.

**Status:** Fixed in B-0 stepping.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.

## 13. IDE Prefetch

**Issue:** While executing a PIO IDE Read Sector(s) or Read Multiple command with PIO pre-fetching enabled, a read of a Non-data Register (such as ALT STATUS Register) may cause the 440MX PIO pre-fetch counter to increment, incorrectly since it should only increment on data transfers.

**Implication:** Invalid data may be written to memory. Due to Intel customers should perform their own risk analysis on this errata and determine the most appropriate work around for their systems.

**Workaround:** Three possible workarounds exist:

1. Do not perform Non-data register reads while an IDE PIO transfer is taking place. In cases where this erratum has been seen, an interrupt (IRQn or SMI) has been used to enter the code from which the ALT STATUS read occurs. Code that is not directly involved in the IDE transfer should not perform the ALT STATUS read to check status of IDE transfers.
2. Use the IDE device idle timer to detect IDE activity.
3. Disable IDE PIO prefetching.

**Status:** Fixed in B-0 stepping.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.



#### 14. PCI Accesses to External PCI-based IDE Devices Will Not Cause Power Management Events

**Issue:** PCI accesses to external IDE devices on the PCI bus do not generate power management events (Idle timer reloads, global standby timer reloads, burst timer reloads, and I/O traps).

**Implication:** Power management of external PCI-based IDE devices must use other means to monitor the activity of those devices.

**Workaround:** System BIOS should use the following methods to monitor external PCI-based IDE devices:

1. If there is a need to monitor accesses to the IDE controller to keep the global standby timer from expiring, the IRQs should be enabled (GRLD\_EN\_IRQ) as a reload event for the global standby timer.
2. If there is a need to monitor an external IDE controller for idleness, use the following algorithm:
  - a. Disable the external IDE controller. Set the 440MX to trap on the IDE access and enable the internal IDE controller.
  - b. When the SMI is generated, the idle timer can be started, the internal IDE controller disabled, and the instruction redone to the external IDE controller. The IDE device is then assumed to be active during idle timer count down.
  - c. When the idle timer times out, an SMI is generated and the 440MX should again be set to trap, the external IDE device disabled, and the idle timer started.
  - d. If the idle timer times out before the trap occurs, then the external IDE controller is idle and can be put into a lower power mode. The 440MX is then set up to trap as in step 3 below.
  - e. If the trap occurs first, the IDE device is not idle. The BIOS then returns to step b above.
3. If there is a need to perform I/O trapping on an external IDE controller, set the 440MX to trap on the IDE access and enable 440MX internal IDE controller. When the SMI is generated, the internal IDE controller can be disabled, the external controller enabled, and the I/O cycle restarted.

**Status:** This will not be fixed in future steppings of the 440MX.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.

#### 15. Bus Master IDE Timeout

**Issue:** During an IDE DMA write, the 440MX IDE controller will invalidate its FIFO if the IDE device deasserts its DREQ signal for greater than 1 us. During the FIFO invalidation, the 440MX does not prevent an FIFO fill from PCI.

**Implication:** In Bus Master IDE (BMIDE) mode, the PCI interface is prefetching data. If this prefetched data gets inserted into the IDE FIFO (during a FIFO invalidation due to DREQ deassertion > 1 us) the IDE controller will lock up. Any future reassertion of the DREQ signal will not be acknowledged by the 440MX IDE controller. BMIDE transactions will not complete on either the primary or secondary channel.

**Workaround:** If the controller locks up, the BMIDE driver must timeout, reset 440MX Start/Stop Bus Master bit, and retry the transfer. Note that this erratum does not occur using PIO mode or Ultra DMA/33 mode.

**Status:** This will not be fixed in future steppings of the 440MX.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.

## 16. Burst Events May Cause LVL2 or LVL3 Register Reads to Be Missed

**Issue:** Burst events that occur after Burst Enable bit (BST\_EN) has been set and before the Processor Level 2 (LVL2) or Processor Level 3 (LVL3) register read may cause the LVL2 or LVL3 read to be missed.

**Implication:** When the above conditions occur, the system will not transition into the Level 2 or Level 3 clock control condition as intended but will remain at full speed.

**Workaround:** Software must ensure that no external burst events are active when placing the system into a LVL2 or LVL3 state. To ensure this, prior to LVL2 or LVL3 register read, only the Device 3 idle timer should be enabled as a burst event. The device 3 idle timer is then enabled with all reload events disabled. The LVL2 or LVL3 register read is performed placing the system into a LVL2 or LVL3 clock control condition. The Device 3 idle timer will then generate a burst event upon expiration. During this first burst, the desired burst events are then enabled. The system then functions as expected.

**Status:** This will not be fixed in future steppings of the 440MX.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.

## 17. Device Trap

**Issue:** When the 440MX has the Device Trap logic enabled for devices 0,1, and 4-13, it forwards the I/O access cycles for the device to the EIO/ISA and IDE Bus.

**Implication:** Accesses to devices in a powered-down state could cause unpredictable results.

**Workaround:** Upon a power-down event for devices 0 and 1 (IDE) the SMI handler must save the IDE register settings in CMOS, disable IORDY, and set PIO transfers for compatible timings. Upon a power-up event for devices 0 and 1, the SMI handler must restore all original IDE register settings and re-initialize the IDE drive to the original Mode (PIO mode or DMA).

Upon a power-down event for all other devices (using EIO), the SMI handler must disable the EIO decode and enable the trap logic for that device. Upon a power-up event, the SMI handler must enable the EIO decode and disable the trap logic.

**Status:** This will not be fixed in future steppings of the 440MX.

**Note:** This erratum was carried over from the *Intel® 82371EB (PIIX4E)*.

## 18. Daylight Savings Time Errata

**Issue:** If the last Sunday in October is the 30<sup>th</sup> or the 31<sup>st</sup> and the daylight savings enable bit is set, the time will not correctly adjust back one hour from 1:59:59 a.m. to 1:00:00 a.m.

**Implication:** The system time may not be correct after the daylight savings time change. The first manifestation of this will be on October 31<sup>st</sup> 1999.

**Workaround:** Three alternative solutions exist:

1. If using Microsoft Windows 95/98 or Windows NT4.0 operating systems, leave the system on and the operating system running at 1:59:59 a.m. on the last Sunday of October. Some operating systems will correctly detect the time change and correct the CMOS time settings.
2. After the daylight savings fallback occurs, change the time manually using either an operating system date/time function or the BIOS setup.
3. Contact your system provider to see if there is a BIOS update available that corrects this condition.

**Status:** Fixed in the B-0 stepping.

## 19. Native Audio Bus Master Base Address

**Issue:** When bit 7 of the Native Audio Bus Mastering Base Address Register is set to 1, accesses to the Native Audio Bus Master Control Registers followed by accesses to the primary codec will only go to the secondary codec.

**Implication:** Since the primary codec can not be accessed it can appear non-functional and the system audio could stop.

**Workaround:** The system BIOS must ensure that bit 7 of the Native Audio Bus Mastering Base Address Register is set to 0.

**Status:** Fixed in the B-0 stepping.

## 20. AC\_RSTB Assertion

**Issue:** AC\_RSTB is asserted when the 440MX is in POS and POSCCL state.

**Implication:** The codec(s) will get cold-reset when the 440MX enters POS and POSCCL states and will lose all of their programming.

**Workaround:** The codec(s) have to be reprogrammed after resuming from POS and POSCCL.

**Status:** Fixed in the B-0 stepping.

## 21. Boundary Condition Issues for USB Connects and Disconnects

**Issue:** Boundary conditions can occur while entering an S1-S5 state. When resuming from POSCL, STR, STD, or SOFF the port enable and port status bits are no longer set. These bits are in the Port Status and Control Register (PORTSC).

The following specifies the boundary conditions that are applicable:

1. If a USB device is *disconnected, connected, and re-disconnected* within 32  $\mu$ sec within a 90 nsec window after the PCI\_STP# signal while entering suspend (S1-S5), it will unintentionally wake up the system and may result in USB instability.
2. If a USB device is *connected, disconnected, and re-connected* within 32  $\mu$ sec within a 90 nsec window after the PCI\_STP# signal while entering suspend (S1-S5), it will unintentionally wake up the system and may result in USB instability.
3. If a USB device is *disconnected, connected, and re-disconnected* that take longer than 32  $\mu$ sec within a window of STPCLK# - 3 PCICLKs but before the clocks resume, while entering suspend (S1-S5), it will unintentionally wake up the system and may result in USB instability.
4. If a USB device is connected and disconnected, and that take longer than 32  $\mu$ sec within a window of STPCLK# - 3 PCICLKs but before the clocks resume while entering suspend (S1-S5), it may unintentionally wake up the system and may result in USB instability.
5. If a USB device is permanently disconnected within a window of STPCLK# - 3 PCICLKs but before the clocks resume while entering suspend (S1-S5), it may result in USB instability.
6. If a USB device is permanently connected, within a window of STPCLK# - 3 PCICLKs but before the clocks resume while entering suspend (S1-S5), it may result in USB instability.
7. If a USB device drives a K state resume after the STPCLK# - 3 PCICLKs and before the clocks stop while entering suspend (S1-S5), which may result in USB instability.

**Implication:** If the conditions above are met, USB instability may result.

**Workaround:** None.

**Status:** The status for each boundary condition is as follows:

1. This will not be fixed in future steppings.
2. This will not be fixed in future steppings.
3. Fixed in the B-0 stepping for the condition before the clocks are suspended, but it will not be fixed while the clocks are stopped.
4. This will not be fixed in future steppings.
5. Fixed in the B-0 stepping.
6. Fixed in the B-0 stepping.
7. Fixed in the B-0 stepping.

## 22. Incorrect Data Transmitted Through AC'97 Modem Out Channel

**Issue:** The following sequence of events may cause incorrect data to be sent out on the AC'97 Modem Out Channel:

1. The AC97 Controller reaches the Last Valid Buffer and the Last Valid Index is updated some time after all the data for the current buffer has been fetched but before it has all been transmitted out.
2. The new buffer starts at an odd word location.
3. The AC97 Controller fetches the new Buffer Descriptor and then fetches the data for the new buffer before the data for the previous buffer (which was the last valid buffer) is sent out on the link.

**Implication:** The AC97controller may send out data from the lower word of the first data fetch in the new buffer instead of the upper word because the buffer is odd word aligned. This problem is seen only on the Modem Out channel resulting in one extra sample being sent out on the link before the new buffer's samples are sent out. Modem drivers that incorporate an error-checking algorithm will see this issue.

**Workaround:** None.

**Status:** Fixed in the B-0 stepping.

## 23. Port Enable/Disable Change Bit Incorrectly Set for OC# Assertion During S1-S5 States

**Issue:** The following applies to OC# assertion:

1. OC# assertion during S1-S2 suspend states will not set the Port Enable/Disable Change bit (USB Port Status and Control Register, bit 3) after resuming from suspend. However, the port will be disabled and the Port Enabled/Disabled status bit (USB Port Status and Control Register, bit 2) will be cleared to 0. The Overcurrent Active bit and the Overcurrent Indicator bit (USB Port Status and Control Register, bits 11:10) will be set correctly.
2. OC# assertion during S3-S5 suspend states will not disable Port Enable/Disable Change bit after resuming from suspend. However, the Overcurrent Active bit and the Overcurrent Indicator bit (USB Port Status and Control Register, bits 11:10) will be set correctly. Note that the occurrence of this boundary condition should be extremely rare since an overcurrent during STR, STD, or SoftOff is not expected.

**Implication:** The Port Enable/Disable Change bit may be incorrect if OC# is asserted during S1-S5 states.

**Workaround:** When exiting from suspend, BIOS should check whether the Overcurrent Active bit and/or Overcurrent Indicator bit is set to "1." If yes, it should take the appropriate actions to respond to an overcurrent event. In addition, if the Overcurrent Indicator bit is set to "1" when exiting from S3-S5, the BIOS should clear the Port Enabled/Disabled status bit to disable the port. The BIOS should not depend on the Port Enable/Disable Change bit to indicate whether the port has experienced an overcurrent event.

**Status:** Fixed in the B-0 stepping.

## 24. Minimum Latency to Access USB I/O Registers After Exiting From Suspend

**Issue:** When resuming from any suspend state in which PCIRST# was asserted (POSCL, STR, STD, or Soft Off), software must wait a minimum of 8 µs after PCIRST# is deasserted before accessing the USB I/O registers.

**Implication:** Invalid states may be read from the USB registers and writes may cause invalid operations.

**Workaround:** When resuming from POS and POSCCL, software must wait 8  $\mu$ s from the deassertion of PCI\_STP# (which allows the system-wide clocks to restart) before accessing the USB I/O registers.

**Status:** This will not be fixed in the B-0 stepping.

## 25. USB Transaction Intimated Without Ample Time to Complete

**Issue:** For the case of two sequential frames, if a transfer descriptor from the first frame is delayed past the **PreSof** point of the second frame, then the transfer descriptor of the second frame is fetched even though it does not have ample time to be executed and completed.

**Implication:** Erroneous data and undefined USB behavior may result.

**Workaround:** None.

**Status:** Fixed in the B-0 stepping.

## 26. Mismatched PIDs Lead to False Bus Cycle

**Issue:** Mismatched PIDs may results under the following sequence:

1. The transfer is an Interrupt/Bulk/Control transfer.
2. The same end-point is being accessed.
3. The data buffer is not D-Word aligned (at an odd address).
4. The two data packets following each other have the same type (data0 followed by data0 or data1 followed by data1).

**Implication:** A false bus cycle is generated by the USB controller on the PCI bus to the data buffer with all byte enables inactive ("1111") and often with invalid data (in the case of an IN transfer).

**Workaround:** The following recommendations should be followed:

1. Do not locate data buffers at non d-word aligned addresses.
2. During this type of transfer always follow a data0 packet by a data1 packet and so on (i.e. do not cause a data toggle error).

**Status:** Fixed in the B-0 stepping.

## 27. Native Modem Bus Master Base Address

**Issue:** When bit 7 of the Native Modem Bus Mastering Base Address Register is set to 1, accesses to the Native Modem Bus Master Control Registers followed by accesses to the primary codec will only go to the secondary codec.

**Implication:** Since the primary codec cannot be accessed it can appear non-functional and the system modem could stop.

**Workaround:** The system BIOS must ensure that bit 7 of the Native Modem Bus Mastering Base Address Register is set to 0.

**Status:** Fixed in the B-0 stepping.

## 28. AC'97 PCM Out

**Issue:** The AC'97 controller in the 440MX will incorrectly insert one extra sample pair on the PCM Out channel under a specific condition. The sequence and conditions are described below.

- The last buffer in the current buffer list has been completely fetched and an odd number of buffers in this list has a length that is not a multiple of four.
- After the last buffer has been completely fetched, software updates the LVI.
- The first buffer in the next current buffer list has a length of exactly six samples.

When this occurs the 440MX will insert one extra sample pair, sent six frames (120 uS) earlier, between the last buffer of the old list and the first buffer of the new list.

**Implication:** The PCM Out channel will distort the intended sound. Since the time between these two buffers represents approximately 20 uS, the added sample should not be noticeable to the human ear.

**Workaround:** None.

**Status:** There are currently no plans to fix this erratum.

## 29. Incorrect Recognition of High/Low Speed USB Device Out of Resume

**Issue:** The USB Port Status and Control Register Low Speed Device Attached bit is incorrectly placed after a full-speed USB device generates K-state to resume system from POSCL, STR, and STD/SoftOff Suspend states. The bit will incorrectly identify the device as a low-speed device. This will only occur when the USB controller is going into suspend and Global Suspend is set before the Port Suspend is set.

**Implication:** Full-speed devices will be incorrectly identified as a low-speed device after resuming from POSCL, STR, and STD/SoftOff Suspend states.

**Workaround:** The workaround is separated into two time periods, before suspend and after resume.

**Before Suspend:** Ensure the BIOS sets the "Port Suspend" (bit 12 of USB IO register 10h/12h) before the "Enter Global Suspend Mode" (bit 3 of USB IO register 0) is set.

### After Resume:

1. Add 20 ms or more delay before the BIOS clears the USB Command register bit 4 (FGR) after system resume from suspend.
2. Clear bit 4 Force Global Resume of USB Command register after resume.
3. Clear bit 3 Enter Global Suspend Mode of USB Command register after resume.
4. Clear bit 6 Resume Detect of both Port Status and Control register after resume.
5. Clear bit 12 of Suspend of both Port Status and Control registers on both ports after resume.

**Status:** There are currently no plans to fix this erratum.

## 30. Power Management General Purpose Status Register "USB\_STS" Bit Not Cleared Correctly

**Issue:** The Power Management General Purpose Status Register USB\_STS bit, bit 8, cannot be cleared after the system is resumed from POSCL, STR, and STD/SoftOff by K-state driven by a full speed USB device under the following conditions:

- When USB Command Register Enter Global Suspend Mode bit (bit 3) is set.
- USB Port Status and Control register Base+10-11h Suspend bit (bit 12) is not set.
- USB Command register Base+00-01h Enter Global Suspend Mode bit (bit 3) is not cleared.
- USB Port Status and Control register Base+10-11h Overcurrent Indicator bit (bit 11) is cleared.
- RSM\_DET bit (bit 6) is cleared.
- Port Enable/Disable Change bit (bit 3) is cleared.
- Connect Status Change bit (bit 1) is cleared.

**Implication:** The 440MX will incorrectly identify that there is a potential wake up event on the USB when in an active state.

**Workaround:** The workaround is separated into two time periods, before suspend and after resume.

**Before Suspend:** Ensure the BIOS sets the "Port Suspend" (bit 12 of USB IO register 10h/12h) before the "Enter Global Suspend Mode" (bit 3 of USB IO register 0) is set.

**After Resume:**

1. Add 20 ms or more delay before the BIOS clears the USB Command register bit 4 (FGR) after system resume from suspend.
2. Clear bit 4 Force Global Resume of USB Command register after resume.
3. Clear bit 3 Enter Global Suspend Mode of USB Command register after resume.
4. Clear bit 6 Resume Detect of both Port Status and Control register after resume.
5. Clear bit 12 of Suspend of both Port Status and Control registers on both ports after resume.

**Status:** There are currently no plans to fix this erratum.

### 31. USB Port Status and Control Register "Connect Status Change" Bit Incorrectly Set

**Issue:** The USB Port Status and Control Register (PORTSC) Connect Status Change bit (bit 1) is not set to "1" when powered on.

**Implication:** The 440MX will not recognize if a device is connected to the USB port.

**Workaround:** When the system is first powered-on, perform host controller reset by setting USB Command Register bit #1.

**Status:** There are currently no plans to fix this erratum.

### 32. USB Rise/Fall Matching Errata

**Issue:** The Specification defines a rise/fall time matching (Trfm) which is calculated by dividing rise time by fall time (Tr/Tf). The specification for a full speed device is 90% minimum and 110% maximum. The 440MX does not meet this specification.



**Implication:** No failures have been reported in system validation to date as a result of this erratum. The 440MX does meet the required output signal crossover voltage specification (Vcrs).

**Workaround:** None

**Status:** There are currently no plans to fix this erratum.

### 33. USB Connect Status Change Bit does not get set under certain conditions

**Issue:** When system is in S0 state with CLKRUN# enabled and PCI bus is idle (and hence STP\_PCI# is asserted), the USB Connect Status Change Bit does not get set.

**Implication:** The USB device will not be detected under the above condition. This may result in a no Plug and Play operation of the affected USB device

**Workaround:** There are two possible workarounds to solve this problem. The description of the workarounds is as follows:

1. Disable CLKRUN\_EN: Clear CLKRUN\_EN Register bit (<PM base>+10h bit 13 clear)
2. Using IO Trap: A BIOS workaround can be implemented using an IO trap mechanism to monitor activities on the USB host controller's port status and control registers.

Register Setup for Workaround using IO Trap:

When CLKRUN# is enabled (<PM base>+10h bit 13 set). Enable device IO trap (Assuming device 12 is used).

- Clear EIO\_EN\_DEV12 (dev7 func3 PCI 5Ch bit 29)
- Set IBASE\_DEV12 (dev7 func3 PCI 68h bits 0-15) to USB base address+10h
- Set IMASK\_DEV12 (dev7 func3 PCI 68h bits 16-19) to 3
- Set IO\_EN\_DEV12 (dev7 func3 PCI 68h bit 20)
- Set <PM base>+2Ch bit 24

Steps for Execution using IO Trap Workaround:

USB host controller port status and control registers (USB base + 10 - 13h) are periodically polled by OS/driver to check for status change. Accesses to these registers are trapped and SMI is generated.

- Confirm the SMI cause is from IO trap of these registers.
- Obtain the Opcode of IO instruction just executed based on the CS:EIP from the SMRAM save state map (translation may be required based on whether the system is running in real, VM86 or protected mode).
- Obtain the data value for the execution of the above IO instruction from the EAX slot of the SMRAM save state map.
- Determine if it is IO read or IO write instruction.
- If it is an IO read instruction, check Current Connect Status (USB base + 10h/12h bit 0).
- If no USB device is connected, no correction is needed.
- If an USB device is connected, check previous connect status flag saved in SMRAM.

- If no USB device was previously connected, it indicates a status change. Correction is needed.
- Patch the data value by setting the Connect Status Change (bit 1).
- Store data value back into the EAX slot of SMRAM save state map.
- Update the previous connect status flag.
- Exit SMI

**Status:** There are currently no plans to fix this erratum.

### 34. **AC97 Soft Audio and Soft Modem Issue during Intel® SpeedStep™ Technology Operating Mode Transitions**

**Issue:** Under certain stress test conditions, occasional system hang may occur during Intel® SpeedStep™ Technology (which is featured in Intel mobile Pentium III processors) operating mode transition while running soft audio or soft modem applications. The AC97 DMA controller is not paused prior to Intel SpeedStep™ technology operating mode transition and there could potentially be memory cycles between AC97 codec and DRAM as the system enters C3 State.

**Implication:** Audio and Modem may show abnormal behavior and the system may hang subsequently.

**Workaround:** The description of the workarounds is as follows. Please contact the Intel Field Sales Representative for the sample code of the BIOS workaround:

**Note:** Modem line drop could potentially occur even with the BIOS w/a. The recommendation is to disable the Intel SpeedStep™ technology operating mode transition if active modem line is detected.

Pause the AC97 DMA controller prior to the Intel® SpeedStep™ Technology operating mode transition to C3 State. The sequence of operation is as follows:

```
GeyservilleTransition PROC    FAR
A transition is needed and okay, save registers we will alter.
Now update the performance control field.
Turn off bus master reload.
Turn off bus master arbiter.
Check if AC97 modem is active. (Dev 0, Func 2, Offset 04h, Bit 0)
Check if Ac97 modem is running (Read AC97 modem controller MBAR and check status of Run/Pause Bit)
Abort transition if modem is active. If not active,
Pause AC97 audio if it is running
Power down AC-link by doing a PR4 command to the codec.
Clear break event status.
Perform Level_3 read to enter C3 state.
Perform SpeedStep™ transition sequence
Transition complete
Restore AC97 in reversed order!
Warm Reset AC97 codec
Restore Register values
```

**Status:** There are currently no plans to fix this erratum.

### 35. GPIO22/PIRQC# and GPIO23/PIRQD# Errata

**Issue:** When GPIO22 and GPIO 23 are selected (PIRQC# and PIRQD# are disabled), it has been observed that interrupts may not be appropriately serviced. It is recommended that GPIO22 and GPIO23 not be enabled.

**Workaround:** Do not select GPIO22 and GPIO23 and use other GPIO pins if needed.

**Status:** There are currently no plans to fix this erratum.

### 36. AC97 Soft Audio and Soft Modem Master Abort Errata

**Issue:** Use of either soft audio or soft modem on an Intel® 82443MX PCISet based platform running a 100-MHz Processor System Bus and an AC97 codec may result in failures. The system continues to function normally while the AC97 hardware may not resume and may require a cold-boot to recover. As a result of the failure, the Master Abort Status bit will be set in the audio or modem function PCI header space. (Bus 0, Device 0, Function 1(audio) or Function 2 (modem), offset 06-07h, bit 13).

**Workaround:** Intel has developed reference code for the workaround. Please contact the Intel Field Sales Representative for the sample code of the AC97 soft audio WDM driver workaround.

**Note:** The workaround needs to be enabled in different places in the driver based on whether it is a WavePCI or WaveCyclic soft audio driver implementation. Also, if it is a WDM soft modem driver, the placement will be different. Conceptually, the workaround remains the same.

The memory allocated by the driver for both the BDL and also the data buffers are marked un-cached. This eliminates write-backs to the soft audio memory locations and hence reduces the frequency of the failure significantly.

To set the memory un-cached after it has been allocated, do the following:

- Save the CR3 register of the processor
- Flush the Translation lookaside buffer (TLB) of the processor
- Detect the paging scheme
- If it is a 4MB paging scheme
  - Get the base address from the CR3 of the processor
  - Convert the physical base address to a virtual address
  - Using the virtual address, traverse to the page directory and set the PCD bit. This will set the entire 4MB page un-cached.
- If it is a 4-KB paging scheme
  - Get the base address from the CR3 of the processor
  - Convert the physical base address to a virtual address
  - Using the virtual address, traverse to the page directory and get the physical base address for the page table entry.
  - Convert the physical base address to a virtual address.
  - Using the virtual address, traverse to the page table entry (PTE) and set the PCD bit. This will set the entire 4KB page un-cached.
- Restore the CR3 register of the processor
- Flush the Translation lookaside buffer (TLB) of the processor
- Invalidate caches and force a writeback (WBINVD).

**Status:** There are currently no plans to fix this erratum.

## ***Specification Clarifications***

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There are no specification clarifications.

## Documentation Changes

### 1. GTL VREF Document Correction for Intel® 82443MX PCISet Electrical and Thermal Specification

The GTL VREF description in the Intel 82443MX PCISet Electrical and Thermal Specification should be changed as described below:

Symbol	Parameter	Min	Max	Unit	Notes
GTL_REF	GTL+ Reference Voltage	$5/9 V_{TT} - 2\%$	$5/9 V_{TT} + 2\%$	V	For Intel® Mobile Pentium® II and Celeron™ (0.25u) designs
GTL_REF	GTL+ Reference Voltage	$2/3 V_{TT} - 2\%$	$2/3 V_{TT} + 2\%$	V	For Intel® Mobile Pentium® III and Celeron™ (0.18u) designs

### 2. PME# Signal Description Correction

The PME# Signal Description is described incorrectly in Table 24 in *Intel® 82440MX PCISet Datasheet* which lists the Power on Reset values for various Signal Groups. PME# Signal is an Input to 440MX during POS, STR and STD and not Driven by 440MX as currently stated.

### 3. Thermal Design Power Change for 66-MHz Operation

The Thermal Design Power (TDP) for 440MX with 66-MHz Operating frequency is 1.7W. The previously stated TDP number, 1.6W, as stated in the *Intel® 82440MX PCISet Datasheet* is incorrect. The TDP for 100-MHz Operating frequency remains unchanged.



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