

# **EtherLink®/MC: Micro Channel Ethernet Adapter Technical Reference Manual**

---

**A member of the EtherLink® product family**

**For 3Com User Group Information  
1-800-NET-3Com**

**Manual Part No. 4354-02  
Published March 1991. Printed in the U.S.A.**

3Com  
Corporation  
5400 Bayfront Plaza  
Santa Clara  
California, USA  
95052-8145

© 3Com Corporation, 1989, 1991. All rights reserved. No part of this manual may be reproduced in any form or by any means or used to make any derivative work (such as translation, transformation, or adaptation) without permission from 3Com Corporation.

3Com Corporation reserves the right to revise this publication and to make changes in content from time to time without obligation on the part of 3Com Corporation to provide notification of such revision or change.

3Com Corporation provides this guide without warranty of any kind, either implied or expressed, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. 3Com may make improvements or changes in the product(s) and/or the program(s) described in this manual at any time.

Use, duplication, or disclosure by the government shall be expressly subject to restrictions as set forth in subparagraph (c) (1) (ii) for restricted Rights in Technical Data and Computer Software clause at 252.227-7013 of the DOD FAR Supp.

# **Contents**

## **Chapter 1: Introduction**

Architecture Overview 1-1  
Modes of Operation 1-2

## **Chapter 2: Functional Description**

Micro Channel Memory Cycles 2-1  
Micro Channel I/O Cycles 2-1  
Micro Channel Setup Cycles 2-2  
Interrupts 2-2  
Local Area Network Coprocessor 2-2  
Packet Buffer 2-3  
Memory Cycle Arbitration 2-4  
Transceiver 2-4  
EtherStart ROM 2-4  
System Configuration Jumper 2-5  
Timing Specifications 2-5

## **Appendix A: Register Definitions**

## **Appendix B: Programmable Option Select**

## **Appendix C: Programming Guide**

## **Appendix D: Memory Utilization Error**

## **Figures**

1-1. EtherLink/MC Adapter Block Diagram 1-1  
2-1. Packet Buffer Memory 2-3

## Chapter 1: Introduction

The EtherLink/MC adapter is a 10 Megabit per second Ethernet adapter designed to be compatible with IBM's Micro Channel architecture.

EtherLink/MC adapter features the following:

- 16-bit data path to and from the Micro Channel
- Shared-memory packet data access method
- 16K on-board packet buffer RAM, expandable to 64K
- EtherStart ROM as an optional feature
- FCC Class B certification
- Complies with UL requirements

## Architecture Overview

The EtherLink/MC adapter is based on the Intel 82586 Local Area Network Coprocessor. On the network side of the 82586, the SEEQ 8023 or AMD 7992 Manchester Encoder/Decoder is used to interface to the transceiver and the AMD 7996 is used as the transceiver chip in the on-board thin Ethernet transceiver. On the host side, the 82586 and the Micro Channel arbitrate for access to the shared 16K packet buffer RAM. Because the EtherLink/MC adapter has only one address/data bus, any Micro Channel cycle directed at the adapter can cause arbitration to occur if the 82586 is active at the time. Refer to figure 1 for a block diagram of the major functional sections of the adapter.

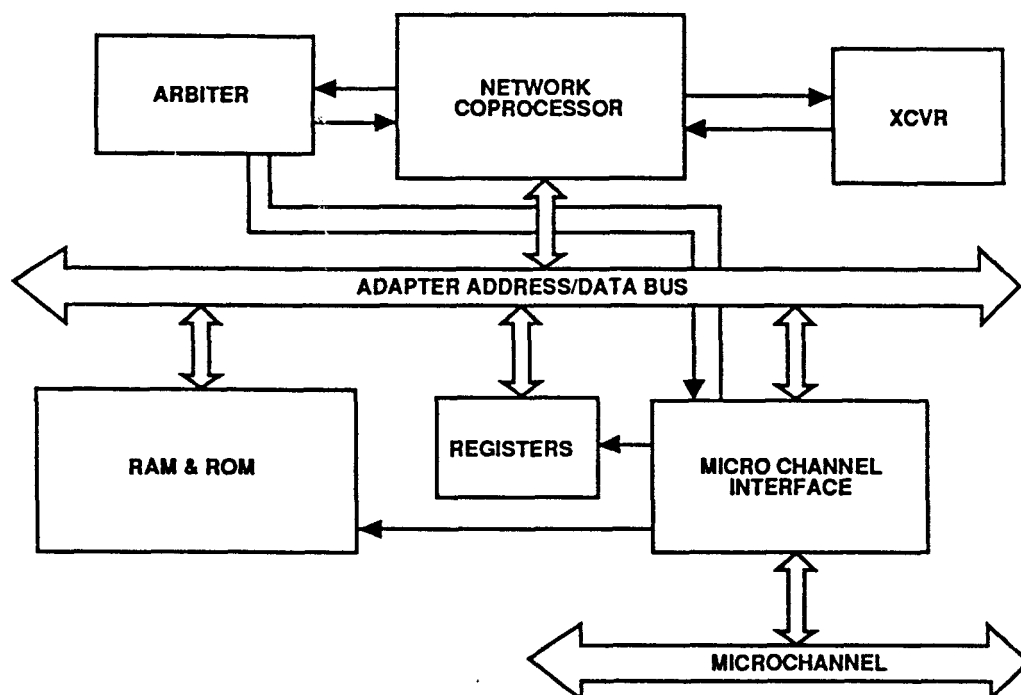


Figure 1-1. EtherLink/MC Adapter Block Diagram

## Modes of Operation

EtherLink/MC adapter has only one significant mode of operation: shared memory. Shared memory allows the adapter to map a 16K window of its memory into the address space of its host. The adapter's memory may be regarded as a specialized extension of the host system's memory. Random reads and writes directed at the shared memory space may take place at any time. Be aware, however, that the 82586 coprocessor also uses this memory and, although transparent to the user, host memory cycles that address the adapter's memory may run slower than system memory cycles because of the need to arbitrate between the host and the 82586.

The only communication path between the host system and the 82586 is through the shared memory. Commands are set up in the shared memory by the host and responses from the 82586 are left in the shared memory for the host to interpret. The host informs the 82586 of pending commands by strobing Channel Attention (described in detail later). Similarly, the 82586 informs the host that it has either completed a command or received a packet by generating an interrupt for the host to respond to.

The EtherLink/MC adapter supports loopback within the 82586 as well as using the loopback capabilities of the Manchester Encoder/Decoder. External loopbacks (functionally equivalent to Encoder/Decoder loopbacks) may also be performed on short packets (18 bytes).

## Chapter 2: Functional Description

This section describes, in detail, the purpose, features and functionality of the several functional sections of the EtherLink/MC adapter.

The EtherLink/MC adapter responds to three different types of Micro Channel cycles. These are: memory, I/O and setup.

### Micro Channel Memory Cycles

EtherLink/MC adapter decodes one of four possible 24K memory address ranges. The base address of these memory ranges are: C0000, C8000, D0000 or D8000. The first 16K of the memory range is dedicated to accessing the 16K window of the adapter's packet buffer RAM. Which of the four 16K banks is accessible through the window is controlled with the +BS0 and +BS1 bank select bits in the Control Register (I/O base + 6). For normal operation of the 16K adapter, +BS0 and +BS1 should both be set to 1 (bank 3). Either 16-bit or 8-bit cycles may be used to access the packet buffer memory.

The last 8K of the memory range is used to access the EtherStart BIOS ROM for booting up the host system using a boot volume from a network resource. The last 8K of the memory range is consumed by the adapter for this purpose regardless of whether or not a ROM is installed in the adapter's EtherStart ROM socket. Though the ROM is only 8 bits wide, the Micro Channel supports 16-bit and 32-bit accesses to the ROM by automatically packing the appropriate number of bytes together to form the desired word. This process is transparent to the host processor.

### Micro Channel I/O Cycles

EtherLink/MC adapter provides four different possible I/O base addresses (0300, 1300, 2300 and 3300). Eight byte-wide I/O registers are designed into the adapter. The first six contain the adapter's unique IEEE network address number (48 bits total). The next register (I/O base + 6) is the control and status register. The last register contains a version number port. The least significant 4 bits of this register contain the current version number. Adapters that contain changes that might affect software will have different version numbers.

All of the I/O registers on the adapter are 8-bit registers. 16-bit I/O cycles to these registers is supported and will result in pairs of registers being selected in sequence.

## Micro Channel Setup Cycles

During Power On Self Test (POST) the Micro Channel accesses special registers on the adapter that identify the adapter type and configure its memory and I/O base addresses, interrupt channel assignment and type of transceiver to be used. These registers are available to be read by drivers and applications to determine the presence and configuration of the adapter. The contents of these registers must not be altered! Only the system configuration utility included in the Reference Diskette for the host machine may modify the contents of the Programmable Option Select (POS) Registers. Only 8-bit accesses to these registers are allowed. Appendix B provides details of the POS registers.

## Interrupts

Interrupts can be programmed to occur under all conditions supported by the Intel 82586. The interrupt status bit in the adapter's Status Register reflects the immediate condition of the interrupt pin on the 82586. This signal is not latched nor is it affected by the state of +INTE (bit 2 of the Control Register). This status bit is intended for diagnostic purposes only and should not be used to determine if the adapter is responsible for generating an interrupt. The 82586's Status Block should be examined to determine if a command that might generate an interrupt has completed its operation.

Once the 82586 activity that generated the interrupt has been acknowledged, the interrupt request line from the EtherLink/MC adapter will be deasserted. Refer to the Intel Microcommunications Handbook for details on interrupts and their acknowledgement.

EtherLink/MC adapter supports open-collector, level-sensed interrupt sharing. Any interrupt handler written for this adapter must also support this protocol. Refer to the IBM Personal System/2 Technical Reference for a discussion on interrupt sharing.

## Local Area Network Coprocessor

The Intel 82586 Local Area Network Coprocessor is used as the interface between the packet buffer, (and therefore the host system) and the Ethernet transceiver. The 82586 receives and transmits network data into and out of the adapter's packet buffer RAM using a "linked-list" method of distributing and assembling packet data.

The 82586 sees the packet buffer as 16K bytes of 16-bit wide memory that resides from C000 to FFFF within its address space (adapters with 64K RAM use 0000 through FFFF). The upper bits (beyond bit 15) of the 82586's address word are ignored. Therefore, the reset vector, normally found at FFFFF6, will actually be stored in the RAM's 00FFF6 location. To the Micro Channel's 16K window, the reset vector looks like it resides at Adapter Memory Base address + 3FF6 of bank 3. See Figure 2 for a memory map of a 16K adapter using the RAM base address of C8000.

The EtherLink/MC adapter is not capable of supporting byte-wide 82586 memory cycles. Therefore, the reset vector structure must specify that the coprocessor operate in the 16-bit mode. In the 16-bit mode, all transfers are 16 bits wide.

## Packet Buffer

The adapter's Packet Buffer is the central point for all operations carried out by the adapter. Transmit and receive buffers and their status words reside in the Packet Buffer. The Packet Buffer is a 16K byte, 16-bit wide static RAM memory. The 82586 sees this memory as 16K bytes installed in its address space from 00C000H through 00FFFFH. After the first Channel Attention following a reset to the 82586, the 82586 will attempt to read location FFFFF6 to fetch the reset vector. Because the adapter's Packet Buffer ignores the upper 8 bits of the 82586's address word, the reset vector should be set up at RAM location FFF6.

The Packet Buffer resides in the first 16K of the 24K of Micro Channel memory address space that the adapter consumes. Relative to the Micro Channel host, the 82586 reset vector should be set up at location C000:3FF6 (assuming a memory base address of 0C0000H) of bank 3.

The Packet Buffer's Micro Channel base address is set by the "RAM" bits in POS register 0 (see appendix B). The 16K segment of the Packet Buffer that is accessible by the Micro Channel is selected by the "BS" bits in the control register (see appendix A). Figure 2-1 shows the mapping of the packet buffer into the 82586's memory space.

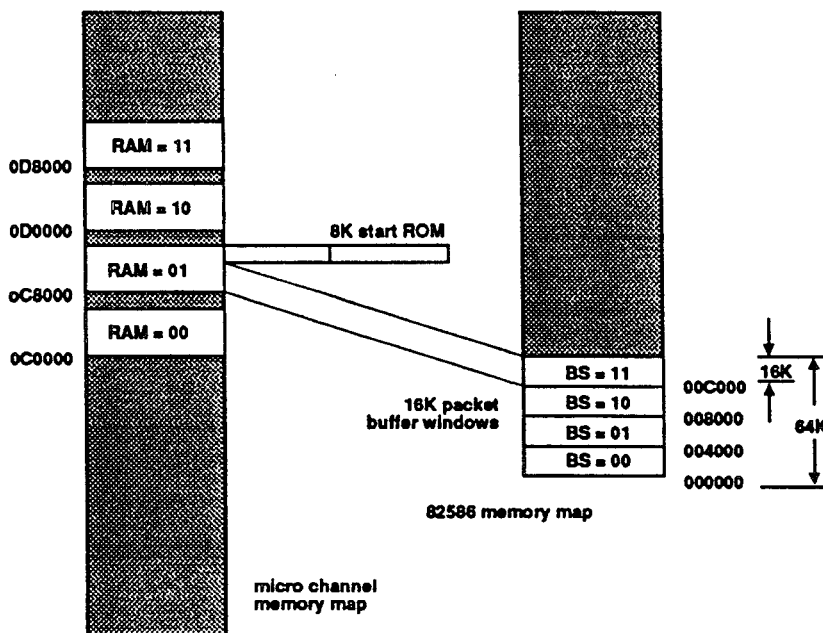


Figure 2-1. Packet Buffer Memory



## Memory Cycle Arbitration

Because two devices (the Micro Channel and the 82586) require access to the same memory, occasional resolutions of conflicts must occur. The adapter's arbitration circuitry is designed to guarantee fair access to the RAM by both requestors.

During Micro Channel to the Packet Buffer when the 82586 is idle, the Micro Channel is allowed free access to the memory and the arbitration circuit does not get involved at all. Similarly, the 82586 has free access to the RAM while the Micro Channel is not using it. However, all 82586 cycles require the assistance of the arbitration circuitry to allow it to access the adapter's address/data bus.

Once the 82586 memory cycle has started, the arbitration circuitry checks, at a particular point in the 82586's cycle, whether or not the Micro Channel is going to be accessing the adapter. If the Micro Channel is indicating activity, the 82586's cycle will be suspended until the Micro Channel has completed its cycle. Once the Micro Channel cycle has been completed, the arbitration circuit claims the adapter bus and allows the 82586 cycle to run to completion.

If the Micro Channel is not indicating adapter activity, the 82586 immediately proceeds with its cycle. During the latter portion of the 82586 cycle, all Micro Channel accesses to the adapter will be deferred until immediately after the 82586 has completed its cycle.

During typical operations, supporting the transfer of continuous 10 Mbit/s of data to or from the adapter will consume approximately 35% of the available bandwidth of a 10MHz 80286 Micro Channel system.

## Transceiver

The EtherLink/MC adapter's transceiver is a 3Com thin Ethernet transceiver. The transceiver is factory tuned and tested to guarantee operation on Ethernet segments that are twice as long as specified by IEEE 802.3.

A control bit in the Programmable Option Select register is provided for "jumperless" selection of either the on-board (BNC) or external (DIX) transceiver.

## EtherStart ROM

A socket is provided on EtherLink/MC adapter for the installation of an optional "EtherStart" ROM. This ROM contains software to allow the Micro Channel system to "boot up" without using local disks. The EtherStart ROM is mapped into the upper 8K of the 24K Micro Channel memory space used by the adapter. Reads from the ROM are byte-wide only. The byte-wide nature of the EPROM cycles is transparent to the programmer and the system. Naturally, execution out of the Start ROM will be slower than execution out of system RAM and, once the boot is complete, all software required by the system should reside in system RAM.

## System Configuration Jumper

There is a single jumper on EtherLink/MC adapter. This jumper is used to allow the adapter to be enabled even though the host system's Configuration RAM contains no entry for the adapter. There is only one condition under which the adapter's jumper should be moved from position "A" to position "B": if the adapter has been installed in a computer that has no floppy disk drives and there is no provision for temporarily installing one to run the configuration utility on the system's reference diskette.

When the jumper is installed in position "B", the Card Enable feature of POS is overridden so that the adapter's Start ROM program can be accessed during the ROM scan that occurs during the power-up sequence. This Card Enable override is necessary when the host system's configuration RAM doesn't contain an entry for the adapter. Without the jumper, if there isn't an entry in the system's CMOS RAM for the adapter, the system will leave the adapter in the disabled state and its ROM won't be found during the ROM scan.

When using the adapter in this specialized configuration, care must be taken that no bus conflicts will occur because the adapter will be enabled before it is configured. The power-up default configuration for the adapter is as follows: I/O base address = 0300H, memory base address = 0C0000H, interrupt level = 12 and the on-board transceiver will be selected.

For general operation, the jumper should be in position "A".

## Timing Specifications

### Micro Channel to/from Packet Buffer

- Basic memory cycle time: 300 nanoseconds

### 82586 to/from Packet Buffer

- Network bit rate: 10.00 Mb/s
- Network data word transfer rate: 1.6 microseconds/word
- Compressed 82586 bus cycle time: 333.3 nanoseconds
- Adapter bus bandwidth consumption: 21%

### 82586 FIFO empty/fill rate

- Maximum 82586 burst transfer rate: 24 Mbps

### Maximum Packet Buffer Access Latency

- Maximum 82586 wait state: 300 nanoseconds
- Maximum Micro Channel wait state: 700 nanoseconds

## Appendix A: Register Definitions

All EtherLink/MC adapter registers are 8-bit registers. Word accesses to a register will result in two accesses occurring to neighboring registers. 16-bit cycles are permitted.

**Register 0: Network Address - byte 0 (Read Only)**

7	6	5	4	3	2	1	0
47	46	45	44	43	42	41	40

**Register 1: Network Address - byte 1 (Read Only)**

7	6	5	4	3	2	1	0
39	38	37	36	35	34	33	32

**Register 2: Network Address - byte 2 (Read Only)**

7	6	5	4	3	2	1	0
31	30	29	28	27	26	25	24

**Register 3: Network Address - byte 3 (Read Only)**

7	6	5	4	3	2	1	0
23	22	21	20	19	18	17	16

**Register 4: Network Address - byte 4 (Read Only)**

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8

**Register 5: Network Address - byte 5 (Read Only)**

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

# A

## EtherLink/MC: Register Definitions

A-2

### Register 6: EtherLink/MC Adapter Control & Status

7	6	5	4	3	2	1	0
-RST	+CA	+LBK	*	+INT	+INTE	+BS1	+BS0

#### Control and Status Register Bits

**+BS+BS(1,0)** RAM Bank Select. (Read/Write) These bits are used to select which 16K bank of the Packet Buffer will be available through the 16K access window. Adapters with 16K packet buffers must select bank 3 for normal operation.

**NOTE:** the power-up condition of these bits is for bank 0 to be selected. This means that until bank 3 is selected the host system cannot access the RAM on 16K adapters.

00 = bank 0

01 = bank 1

10 = bank 2

11 = bank 3 (Required setting for 16K adapters)

**+INTE** Interrupt Enable. (Read/Write) This bit is set when it is desired to have the 82586's interrupt line generate a Micro Channel interrupt. For normal operation it is not necessary to ever clear the +INTE bit. Proper use of the 82586 will prevent the generation of interrupts. The +INTE bit should generally be set and only cleared for diagnostic or development applications.

**+INT** Interrupt Active. (Read Only) This status bit is set when the 82586 asserts its interrupt line. This status bit is not latched and reflects the immediate condition of the 82586's interrupt line. Use of this bit is intended primarily for diagnostic and/or development applications.

**+LBK** Loop Back Enable. (Read/Write) Setting the Loop Back bit causes the Manchester Encoder/Decoder to enter the loopback mode. This bit must be cleared to a zero for normal network operation.

**+CA** Channel Attention. (Read/Write) Writing a one to this bit asserts the channel attention signal to the 82586. This bit must be reset to a zero no less than 500 nanoseconds after it was set. Because the 82586 responds to the falling edge of Channel Attention, it is recommended that it be deasserted as soon as possible after the minimum time has elapsed in order to minimize 82586 response time.

**-RST**      82586 Reset. (Read/Write) Clearing this bit will assert the 82586's RESET line. The 82586 will remain in the Reset state as long as the -RST bit is low. This bit is low upon power-up.

**NOTE:** the 82586 is also reset as long as the adapter is in the "disabled" state (see Appendix B).

**\***      Reserved. This bit is reserved for future use. Readings of this bit are undefined. This bit should be set to zero for normal operation of the adapter.

**Register 7: EtherLink/MC Adapter Revision Level**

7	6	5	4	3	2	1	0
*	*	*	*	+RL3	+RL2	+RL1	+RL0

**+RL(3, 0)**      Revision Level. (Read Only) These four bits are available to indicate the software compatibility revision level of the adapter. The initial version of the adapter's revision code was F (hex). The gate array version of the adapter uses revision code E hex.

**\***      Reserved. These bits are reserved for future use. Readings of these bits are undefined. These bits should be set to zero for normal operation of the adapter.

## Appendix B: Programmable Option Select

The Micro Channel architecture supports “jumperless” reconfiguration of adapter options such as interrupt levels and base addresses. During Power On Self Test (POST), the Micro Channel will use the contents of the host system’s battery-backed CMOS configuration RAM to program the adapter’s POS registers.

The Micro Channel reads I/O locations XXX0H and XXX1H while in the “setup” mode to determine the adapter ID code. EtherLink/MC adapter responds with 6042H. If a match is made in the CMOS RAM, the programming of the POS registers proceeds.

**Register 0:** Location XXX2H

7	6	5	4	3	2	1	0
+IFBK1	+IFBK0	-BNC	+RAM1	+RAM0	+ARA1	+ARA0	+CDEN

**+CDEN** Card Enable. (Read/Write) This bit is set when the adapter has been enabled by the POST routine. Generally, when the +CDEN bit is cleared, the adapter will only respond to setup operations. It is possible, however, for the adapter to be enabled even if this bit indicates that it shouldn’t be. If the adapter’s Network Address isn’t being read as all FFs and the +CDEN bit indicates that the adapter shouldn’t be enabled, then the adapter’s System Configuration jumper is in position “B”. This determination may be useful for certain implementations of network start software ROMs.

**+ARA(1, 0)** Adapter Register Address. (Read/Write) These bits indicate where in the Micro Channel’s 64K I/O space the adapter’s registers will reside.

00 = 0300  
01 = 1300  
10 = 2300  
11 = 3300

# B

EtherLink/MC:  
Programmable  
Option Select

B-2

**+RAM(1, 0)** Memory Mapped RAM/ROM Base Address. (Read/Write) These two bits select where the 24K memory space of the adapter (16K RAM, 8K ROM) will be mapped into the Micro Channel's memory space.

00 = 0C0000

01 = 0C8000

10 = 0D0000

11 = 0D8000

**-BNC** On-Board Transceiver Enable. (Read/Write) Clearing this bit enables the on-board thin Ethernet transceiver.

**+IFBK(1, 0)** Interrupt Channel Select Feedback. (Read Only) These bits indicate which interrupt channel has been assigned to 82586 operations.

00 = 12

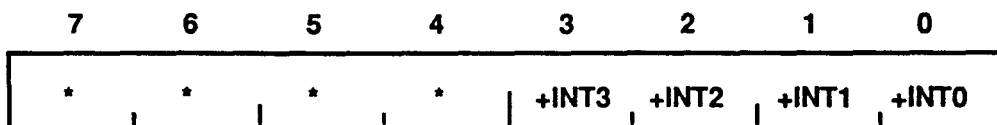
01 = 7

10 = 3

11 = 9

**NOTE:** It is possible for the POST routine to incorrectly set the interrupt level. It is, therefore, recommended that when determining the configuration of the adapter, drivers should read the feedback bits +IFBK(1, 0) and then write the corresponding interrupt select code to location XXX3H while in setup mode. No other configuration registers should ever be (or ever need to be) written to by drivers or applications.

**Register 1: Location XXX3H**



**+INT(3, 0)** Interrupt Level Select. (Write Only) The lower four bits of this register are used to select one of four possible interrupt channels (or levels) for use by the 82586. Each bit corresponds to a separate interrupt channel.

0001 = 12

0010 = 7

0100 = 3

1000 = 9

## Appendix C: Programming Guide

This section presents several general guidelines and explanations of various less-than-obvious characteristics of the design.

- Both the POS registers and the control register at I/O base address + 6 are cleared during power-up or at any time that the system processor asserts the +CHRESET signal.
- After a reset, the on-board transceiver is enabled. If so configured by the user, the POST routine will turn off the transceiver and select the DIX connector.
- Both the 82586's RESET line and Channel Attention line require deliberate action by the host to deassert them. Neither of these signals generate automatic strobes when set.
- A version number of the adapter can be obtained by reading location I/O base + 7. Version numbers will be used to differentiate between the initial adapters and future versions that may contain enhancements. Proper use of the information provided by the version number will allow the latest version of driver software to work with all versions of the adapter while taking advantage of advancements and improvements made to later adapters.
- The configuration of the adapter after POST can only be reliably determined by reading the adapter's POS registers. Do not attempt to interpret the data stored in the host system's battery-backed CMOS RAM.



## **Appendix D: Memory Utilization Error**

Early production units of the EtherLink/MC adapter contained a memory allocation error. When configured to use I/O base address C8000 or D8000, the adapter responds through a 32KB range, resulting in a double appearance of the start PROM in host memory, which may cause the adapter to malfunction. Normal network operation is unaffected. The problem has been solved on subsequent production boards.